Perspective of RPC PAC trigger operation at high luminosity

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Electronics aging

- The Link System (UXC) and Trigger System (USC) were produced on 2006-2007. So after the LS2 (2019) it will be ~12 year old. It works in principle non stop since the installation (2008)
- I talked to our engineers, it is very hard to give any strict estimation of the electronics life time.
- I googled a little. Here what I found:

  Altera Reliability Report 52
  http://www.altera.com/literature/rr/rr.pdf?GSA_pos=1&WT.oss_r=1&WT.oss=Altera

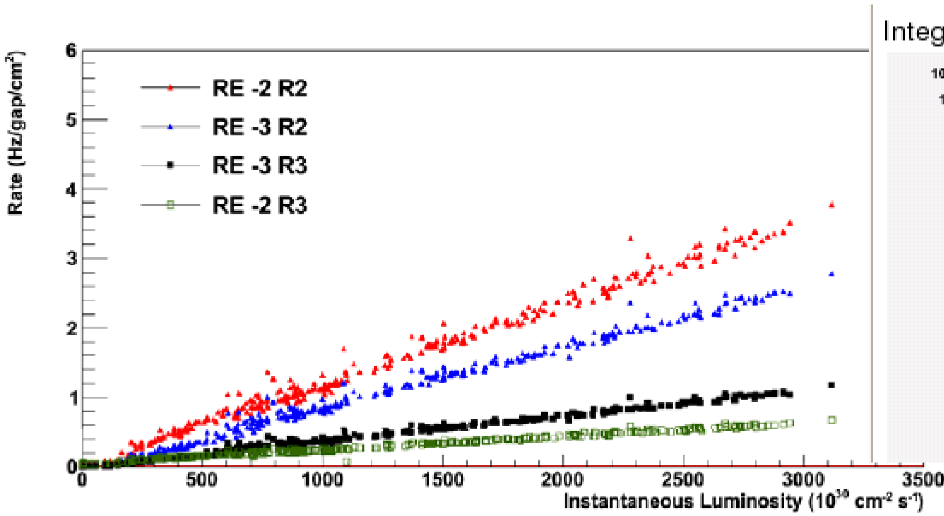
  For the Stratix II (PAC chips and other Trigger Board chips) it report 22.9 FITs – lower limit (no failures observed in the tests).

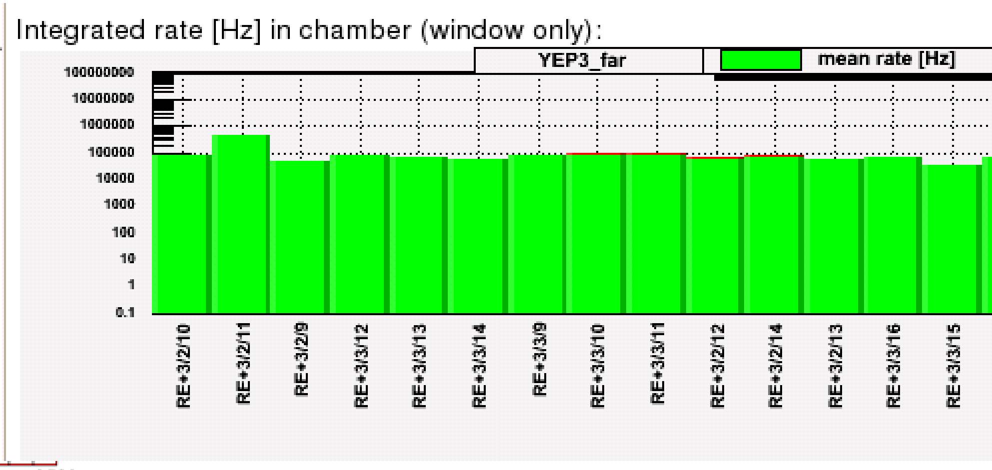
  FITs or Failures In Time, where one FIT is equivalent to one failure in one billion or **10^9 device-hours.**
  We have about 500 such devices, so 10 years is ~$5*10^7$ device-hours.

Link System – radiation effects

- The Link System (Link Boards and Control Boards) are exposed to the radiation. They are placed on the detector balconies where the radiation levels are relatively low.
- Two effects should be considered:
  - **Single Event Upsets** (transient changes of single bits in the memories).
    The probability is linear with the radiation level. During last year we observer only a few SEU-like problems. But in fact it could be much more of them – we are not able to detect the SEU directly by the firmware readback.
    If the SEUs induced problems are too frequent, we can increase the rate of the Hard Reset (periodic firmware reloading). Now it is performed every 30 minutes.
  - **Total Ionizing Dose effects**
    - We have not tested the FPGA we are using on the link system (Xilinx Spartan 3) against the TID effects. Not easy to find data for that particular devices.
      What I found: "Total Ionizing Dose Performance of SRAM-based FPGAs and supporting PROMs" by Joe Fabula and Howard Bogrow, gives the that various Xilinx devices are **"usable in applications up to 60-100 krads(Si)"**.
      On the balconies we can expect for 10 LHC years with nominal luminosity **below 100 rad** (1Gy).
    - We tested the FLASH memories, their survived the dose that exceeds a few times the expected doses.
    - Beside the Xilinx Spartan and FLASH memories we are using CERN rad-hard AISICs: TTCrx, QPLL, CCU25, so for them radiation on the balconies should not be a problem.

Link System performance v.s. chamber occupancy





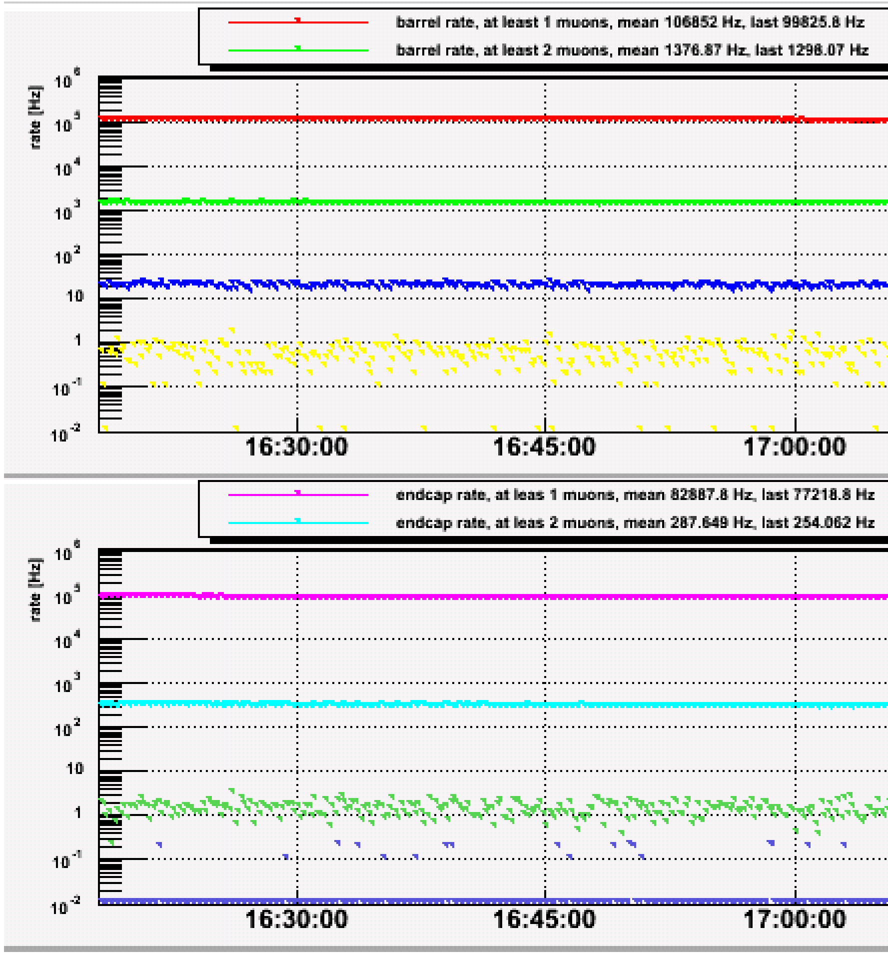
- **@ L=4.5e33 cm^{-2}s^{-1}** the rate in RE3 chambers is up to **100 kHz/chamber** when each fired strip is counted.
- One optical link transmit data from 3 chambers, but clusters (hits) are important not the fired strips, then we have **150 kHz /link (**as the cluster size is ~2).
- Scaling to L=1e35 cm^{-2}s^{-1}
  rate per link 3 MHz/link = almost 1 hit / 10 BX
- With this rate the fraction of hits lost due to the link bandwidth overflow is **< 10^{-6}**
  - assuming Poison distribution of hits per BX, i.e. not taking into account showers (punch throughs).

Trigger electronics performance in high luminosity

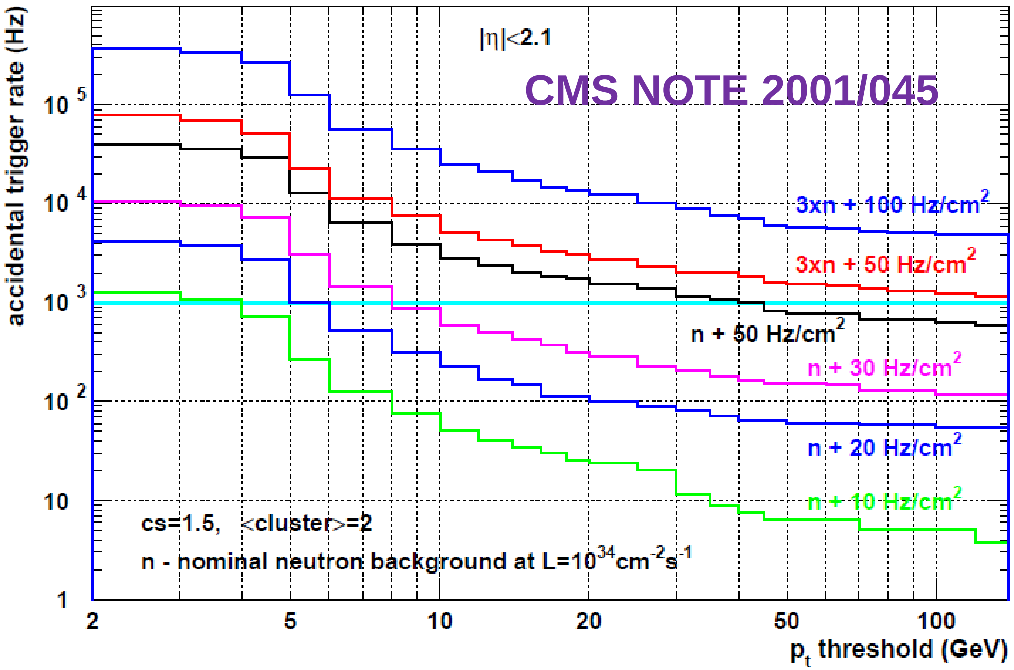
- @ L=4.5e33 $cm^{-2}s^{-1}$ the output PAC candidates rate is:
  - ~100 kHz in barrel
  - ~80 kHz in endcaps

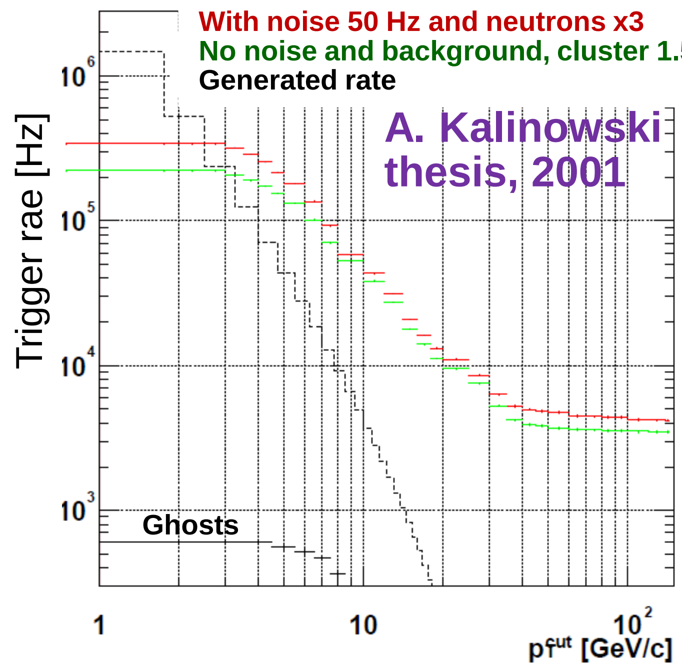
  In the trigger electronics in principle there are no limits on the trigger rate from the transmission bandwidths or processing algorithms.

  The only limit is 4 barrel + 4 endcap candidates / BX



Trigger algorithm performance vs. background rate –false candidates



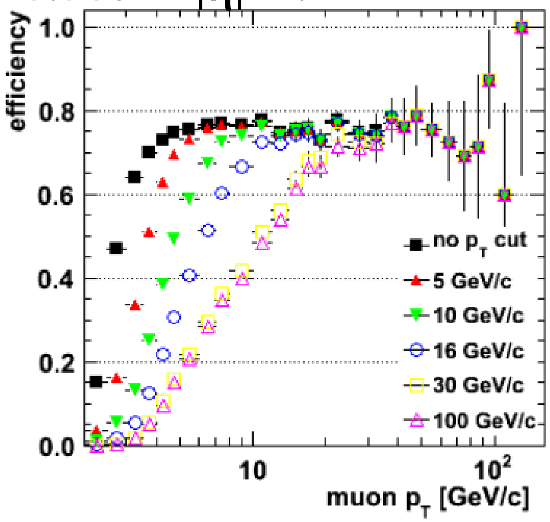


Coincidence of the background hits can give false muon candidate. The effect depends strongly on the PAC algorithm – on the above plots the "4 out of 6" algorithm is used, while now we have in the b.arrel "3 out of 6".

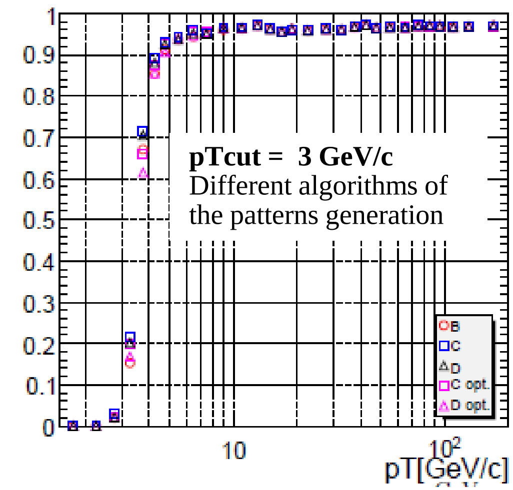
If the background hit is close to the muon hits, the higher pT pattern can fit to the track than without such a background hit. I have no data that estimates this effect

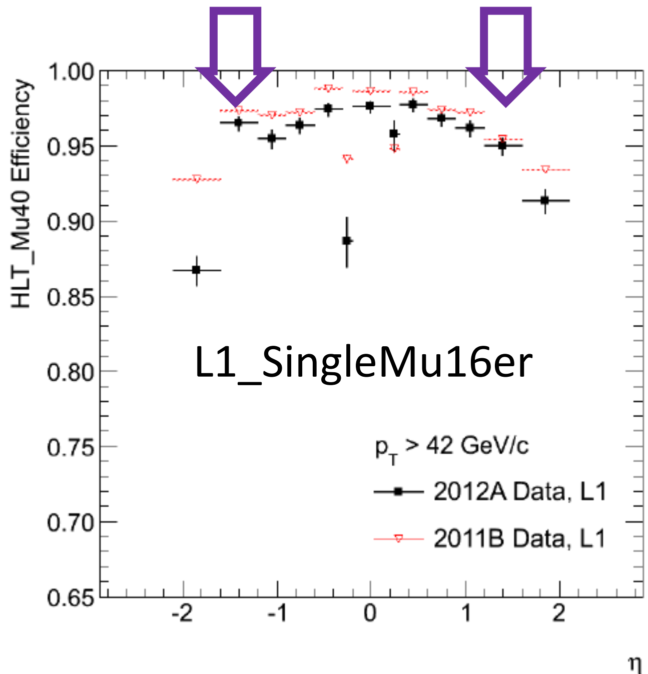
RPC trigger efficiency with out / with RE4

Current RPC trigger efficiency in the endcaps (3 layers) **from data**: **75.9% in |η|>1.24**



RPC trigger efficiency in the endcaps with the RE4, "3 out of 4" algorithm, all possible 3/4 combination allowed (**old Monte Carlo**): **~95% in trigger tower 10**





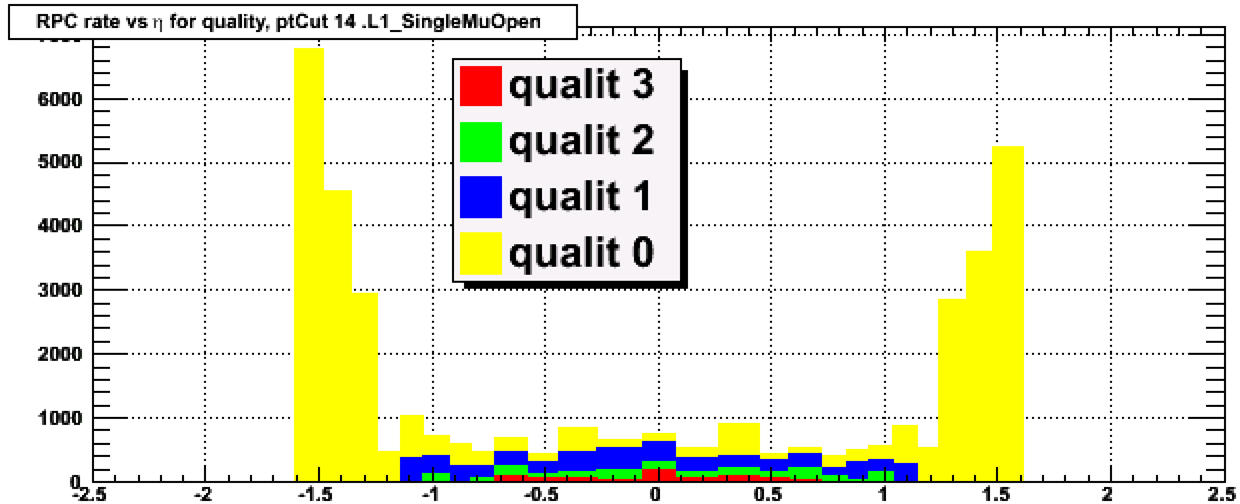
The L1 efficiency in the region 1.2 < |η| < 1.6 is relatively small, with RE4 should be increased.

Muon HLT meeting, Sinead Walsh

https://indico.cern.ch/materialDisplay.py?contribId=2&materialId=slides&confId=173145

Trigger rate

Current RPC trigger rate (3 layers) **from data**,
The rate in the endcaps towers is already ~10 times higher than in the rest of the system



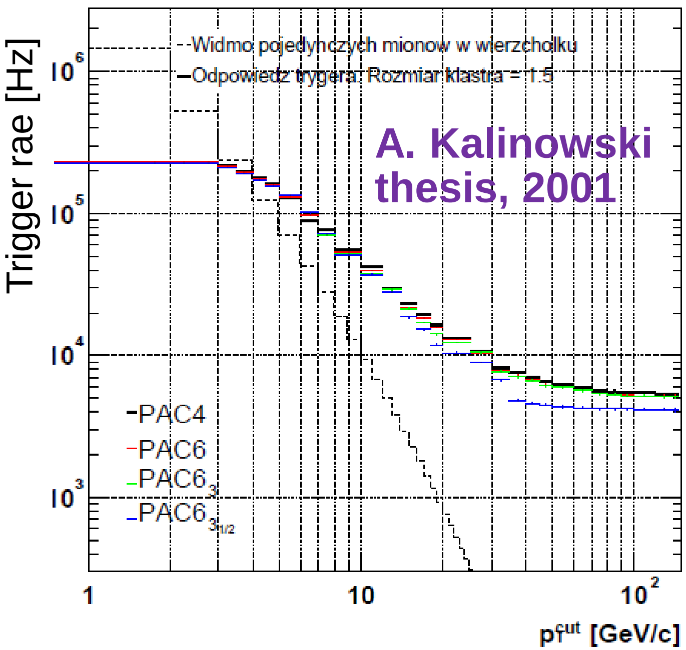
The impact of including the RE4 on the PAC trigger rate is not obvious:

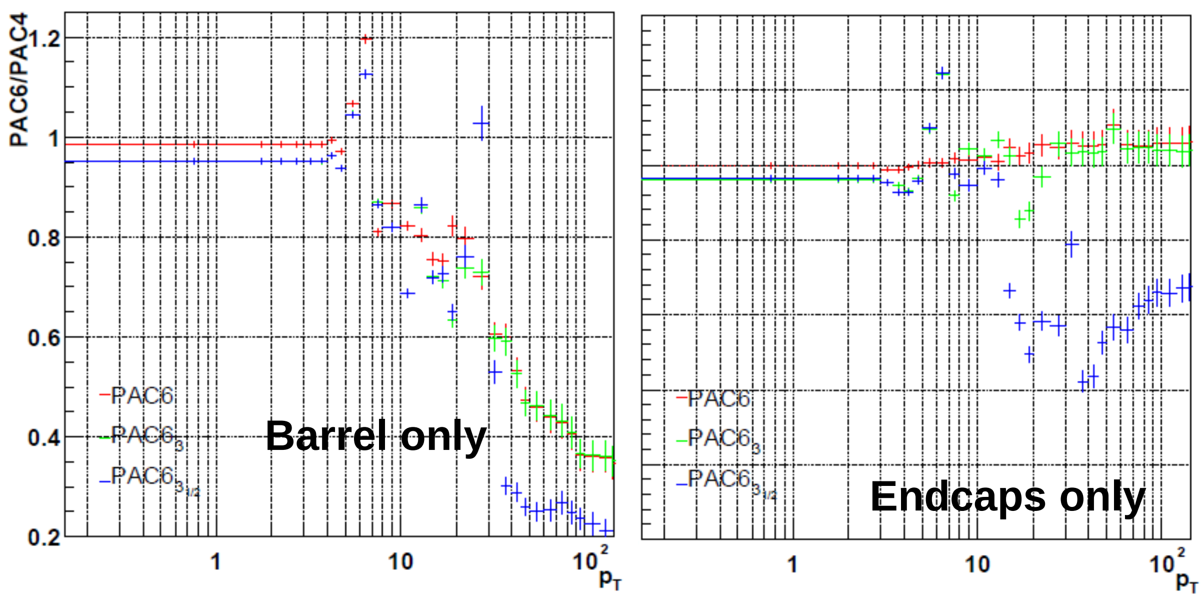
- In that region the Δφ between the station 1 and 2 is very small, and between the station 2 and 3(4) is dominated by the multiple scattering,
- the 4/4 coincidence should give better pT estimation ⇒ smaller rate
- but the 3/4 coincidence without 1st and 2nd station have tendency to overestimate the pT ⇒ bigger rate. But such tracks can be suppressed by the GMT/GT.
- The rate can be controlled by patterns optimization (by the price of efficiency).
- **The cluster size has very big impact on the trigger rate (with big clusters the hits more likely fit to the high pT patterns)**

The impact on the L1 rate is even less obvious – depends e.g. on GMT algorithm (which is under discussion now)

De-clusterization

- In the PAC chip we can implement the de-clusterization to improve the resolution of the RPC hits and thus the pT resolution of the trigger:
  - Simplest option – reject tow extreme strips in the cluster, e.g. if the cluster has size 3, leave only the middle strip fired.
  - More advanced option – define the patters on “half-strips” – $PAC_{1/2}$





Relative rate reduction for different PAC algorithms

New PAC chips

- The PAC FPGA chips are placed on the mezzanine boards, so it is relatively easy to replace them with new, bigger chips.
- At the moment we are using **Altera Stratix 2** (EP2S60 in the barrel, EP2S30 in the endcap; 2005 technology),
  300 chips are needed to cover full detector**.**
- Last year we did an exercise to build a mezzanine with new **Altera CYCLONE IV (EP4CE115F23I7) FPGA (~4 times bigger then the current ones; budget line).** The mezzanine was working with the current Trigger Boards without problems.
- Bigger FPGAs would allow to implement more patterns or more sophisticated algorithms, e.g.:
  - Do chamber hits de-clustering $\Rightarrow$ better pt resolution = smaller rate
  - HSCP triggering with 25 ns bunch spacing

Conclusions

- The PAC trigger system was build such that it exploits entire potential of the RPC detector. The are no week points in the trigger system that deteriorate its performance

  ⇒ there is no big room for improvement
- Optimizations of the PAC algorithm are possible, as it is implemented in the FPGAs. If the PAC chips are too small for the new algorithm, they can be changed to bigger one.
- The simulations of the trigger performance with the RE4 are needed.
- Studies are needed to evaluate the performance of the PAC trigger at the high luminosity LHC.
- The aging of the trigger electronics can be an issue (originally it was planed to exchange the entire L1 trigger electronics after ~10 years of operation).
- The high-eta region is not discussed in this talk – most probably it must be completely new system.
- The idea of building new muon trigger incorporating data from all 3muon subsystems will be discussed in the the my talk in the plenary session.

Backup

RE4 re-scope – improvements in the endcap performance

- The RE4 should allow to increase the RPC PAC trigger efficiency in the **$1.24 < |\eta| < 1.61$** (trigger towers 10, 11, 12) from **76% to ~95%**, and to have redundancy in case of failing chambers.
- The impact on the trigger rate is not obvious, but by tuning the trigger algorithm and patterns set it is possible to control the rate. The cluster size has significant impact on the trigger rate.
- The simulations of the trigger performance with the RE4 are needed.
- The Trigger hardware in the USC is ready for the RE4, no hardware changes are needed.
- The Link and Control Boards for the RE4 are being produced by the Napoli group.